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Amendments to the Claims

1. (Currently Amended) A semiconductor device comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon deposited over the first oxide layer;

an inter-layer insulation deposited over the first polysilicon layer;

a second polysilicon layer deposited over the inter-layer insulation; and

a deposited phosphorous-doped oxide layer provided along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

2. (Original) The semiconductor device of claim 1, wherein the first oxide layer is a tunnel oxide layer.

3. (Original) The semiconductor device of claim 1, wherein the inter-layer insulation is an oxide nitride oxide layer.

4. (Original) The semiconductor device of claim 1, wherein the first polysilicon layer is a floating gate.

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5. (Original) The semiconductor device of claim 1, wherein the second polysilicon layer is a wordline.

6. (Currently Amended) A semiconductor device after re-oxidation comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon layer deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a deposited phosphorous doped oxide layer provided along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous doped oxide layer extending no higher than the second polysilicon layer; and

a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.

7. (Previously Amended) The device of claim 6, wherein the height is a vertical distance from the source to a bottom edge of the first polysilicon layer and the width is a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide layer, wherein

the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide layer.

8-12. Canceled.

13. (Currently Amended) A computer system comprising:

at least one processor;

a system bus;

a flash memory device coupled to the system bus, the memory device including one or more flash memory cells comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon deposited over the first oxide layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a deposited phosphorous doped oxide layer provided along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer; and

a re-oxidation oxide profile formed over surfaces of the semiconductor device having a height and width.

14. (Currently Amended) A self aligned source of a flash memory device on a substrate, the self aligned source comprising:

a horizontal layer planar to the substrate having a first doping concentration;

a vertical layer perpendicular and coupled to the horizontal layer, the vertical layer having a second doping concentration lower than said first doping concentration; and

a deposited vertical phosphorous-doped oxide layer provided only on the vertical layer, the vertical phosphorous-doped oxide layer having a third doping concentration, said self-align source having a resistance less than a similarly doped self aligned source without the vertical phosphorous-doped oxide layer due to a more uniformed doping concentration throughout the self aligned source, thereby permitting a deeper trench depth between adjacent self-aligned sources ~~deeper~~ than ~~the~~ similarly doped self aligned sources without the vertical phosphorous-doped oxide layer.

15. (Previously Presented) The self aligned source of claim 14, wherein the third doping concentration and the second doping concentration produce an effective doping concentration substantially equal to the first doping concentration..

16. (Previously Presented) The self aligned source of claim 14, wherein the third doping concentration is selected from a range from about 1% to about 6%.

17. (Previously Amended) The self aligned source of claim 14, wherein the vertical phosphorous-doped oxide layer has a thickness selected from a range of about 25Å to about 500Å.

18. (Previously Amended) The self aligned source of claim 14, wherein the third doping concentration and a thickness of the vertical phosphorous-doped oxide layer are selected to achieve desired characteristics of the flash memory cell, said desired characteristics include program rate, ease rate, and data retention.

19. (Currently Amended) A semiconductor device comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon deposited over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer; and

a deposited phosphorous-doped oxide layer provided along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

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20. (Currently Amended) A semiconductor device after re-oxidation comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source;

a first polysilicon layer deposited over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a deposited phosphorous doped oxide layer provided along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer; and

a re-oxidation oxide profile having a width defined by a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the first oxide layer, wherein the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide layer.

21. (Currently Amended) A semiconductor device after re-oxidation comprising:

a substrate;

a drain formed in the substrate;

a self-aligned source formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source, said first oxide layer having a first thickness;

a first polysilicon layer deposited over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer deposited over the first polysilicon layer;

a second polysilicon layer deposited over the second oxide layer;

a deposited phosphorous doped oxide layer provided along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer; and

a re-oxidation oxide profile adjacent said self-aligned source having a width defined by a horizontal distance from a side edge of the first polysilicon layer to a point where said first oxide layer starts to get thicker than said first thickness, and a height defined by a vertical distance from a top surface of said self-aligned source to a bottom edge of said first polysilicon layer, wherein the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide layer, and said height is higher than a re-oxidation profile height without the phosphorous doped oxide layer.